REVIEW OF LOW POWER LFSR DESIGN TECHNIQUES

Simoni Shah
Department of Electronics and Communication
Vishwakarma Govt. Engineering College
Ahmedabad,Gujarat,India

Anuj Gundani
Department of Electronics and Communication
Vishwakarma Govt. Engineering College
Ahmedabad,Gujarat,India

Jayesh Diwan
Department of Electronics and Communication
Vishwakarma Govt. Engineering College
Ahmedabad, Gujarat,India

ABSTRACT

Nowadays in the VLSI domain, testing has become inextricable due to the increasing number of transistors on a chip. On the other hand, the chip area is decreasing vastly and low power consumption has become one of the top priorities in testing the chip as well as in the normal operation of the chip. Several techniques to test the chip have been introduced since the 1940s and the evolution of new and efficient testing techniques is increasing day by day. Out of the three methods discussed, the Low Transition LFSR method achieved Low consumption of power in a 32-bit pattern generator using LFSR and reduced switching activity between the test vector. In the Sub-threshold method, four different LFSR architectures are proposed using a combination of different D-Flipflop like true-single phase clock (TSPC) and transmission gate based with X-OR gate (static CMOS or Transmission gate). Moreover, another method using LFSR based on a multiplexer, specially designed for low power Design for Testability (DFT) approaches to EX-OR the single input change patterns generated by a counter and a gray code generator.

Keywords— low power, testing, LFSR.

1. INTRODUCTION

According to Moore's law, the density of transistors on the chip is increasing exponentially every 1.5-2 years. With increasing density manufactures of VLSI chips are mainly concerned about high speed, low size, and minimum power consumption. VLSI technology is currently functioning in nanometre and is aiming to reduce power consumption especially while testing the chip. High power dissipation results in heat loss and apparently to data loss. Conventionally, various testing techniques are being used like ADHOC, BIST, exhaustive etc. These techniques use LFSR to generate a random pattern that is fed to the circuit as input and examine the output.

Section 2 gives the brief about types of power consumption in a chip and LFSR, Section 3 discusses three different LFSR techniques aimed to reduce power, Section 4 draws a comparison between those techniques and shows simulation results and Section 5 gives the conclusion of this paper.

I. POWER CONSUMPTION & LFSR

A. Power Consumption

Power consumption and LFSR:
Mainly power consumption is of two types:
1) Static power or leakage power
2) Dynamic power or switching power

In smaller geometries i.e less than 90nm, leakage power is dominant whereas in larger geometries switching power is more dominant. Various techniques try to incorporate power reducing strategies.

Total power dissipation in CMOS is a function of switching activity, capacitance, voltage, and the transistor structure itself. Charging and discharging of capacitances in the circuit results in switching power dissipation. In any instance when gate switches state, there is a direct connection between the Vdd and ground, resulting in a short-circuit current.

$\mathbf{P_{(switching)} = a.f.\ Ceff.Vdd^2}$
a = switching activity,
f = switching frequency
C_{eff} = the effective capacitance
V_{dd} = the supply voltage.

$\mathbf{P_{(short\text{-}circuit)} = I_{sc}.V_{dd.}}$
I_{sc} = the short-circuit current during switching.

Controlling the switching activity, clock frequency, and also by reducing capacitance and V_{dd} can result in the reduction of dynamic power.

Also, the equation of leakage power is:
$\mathbf{P_{(Leakage)} = f\ (V_{dd},\ V_{th},\ W/L)}$
V_{th} = the threshold voltage,
W = the transistor width,
L = the transistor length.
Leakage power is because of the leakage current.

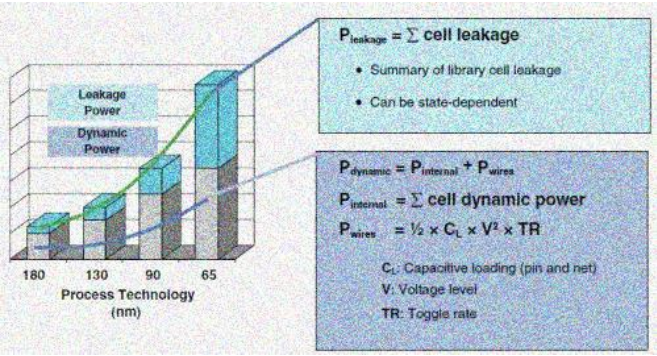


Fig.1 Graphical representation of leakage power and dynamic power in nanometer technology

B. LFSR

LFSR has vast applications in VLSI such as in DFT (Design for Testability), cryptography etc. A simple structure of LFSR is presented here. LFSR generates pseudo random patterns for testing. It is made up of several D - flipflops and an ex-or gate or ex-nor gate. The first input pattern fed to the circuit is known as seed. The first input cannot be 0000 if EX-OR is used and 1111 if EX-NOR is used.

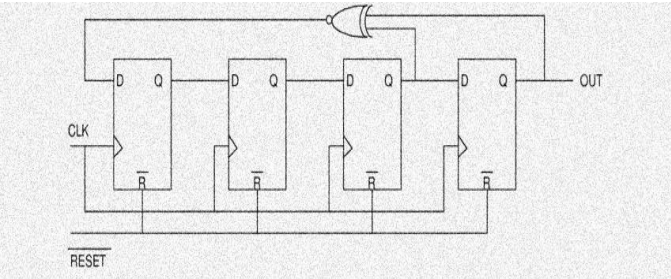


Fig.2. LFSR Structure

II. DIFFERENT LOW POWER LFSR TECHNIQUES

A. Low Transition LFSR

[1] Proposed a method to reduce the transition between two successive test pattern inputs i.e. the switching activity by injecting intermediate patterns. The given method can be used for both combinational and sequential circuits. The power consumed can be reduced by reducing the switching activity between unique test pattern generators. The normal architecture of LFSR is revised such that intermediate patterns can be injected between the two input patterns. The above-mentioned idea is implemented by two schemes:

1)Random injection (RI)
2) Bipartite LFSR

The above two schemes are discussed in detail in the presented paper with example. In Random Injection a new test vector P+ is inserted between two successive test vectors P1 and P2. The transition between P1 and P+ and between P+ and P2 is less than the transition between P1 and P2 separately.

P1:

1	0		0	1	0	0	0	1	1	1	0	1	0	1	0	1

P+:

1	R	0	R	R	R	0	R	R	1	0	R	0	1	0	R

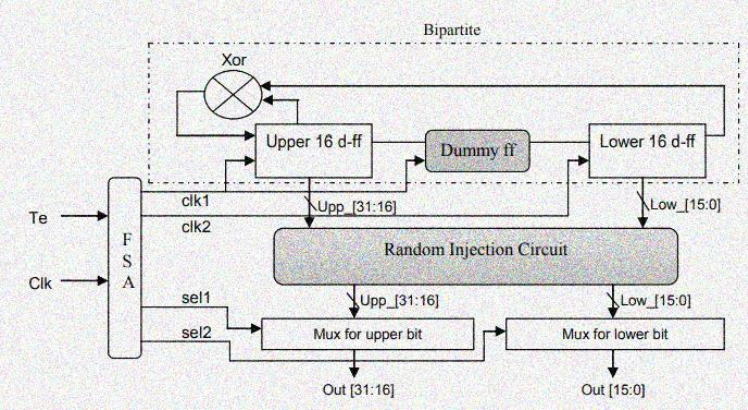
P2:

1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0

Fig.3.1 Example of RI Injection

As shown in figure the transition can be reduce by putting RI in between. We can put R= 0 or 1, as per the requirement.

In Bipartite LFSR two non-overlapping clocks are used to separate LFSR into two equal parts i.e. when one half of the LFSR is working the other half is deactivated and vice versa. The described process is explained in detail with example and steps. The simulation results are obtained in Xilinx 13.1 ISE design suite using Verilog HDL.



B. Sub Threshold

[2] proposed to use the advantage of digital subthreshold circuits that achieve minimized power consumption. In the subthreshold region, the transistors operate with the supply voltage (V_{DD}) less than the transistor threshold voltage (V_{TH}). The equation of operating current in the subthreshold region:

$$I = I_0 \frac{W}{L} e^{\frac{Vgs-Vth}{nV_t}} \left[1 - e^{\frac{-V_{Ds}}{V_L}}\right]$$

The proposed design uses LFSR in subthreshold regions. The conventional LFSR is made up of D-FLIPFLOP (used as shift registers) and EX-OR/EX-NOR gate (used to send feedback). The presented paper explains in detail two different architectures for both D-Flip Flop and X-OR gate. The two discussed architectures for D-Flip Flop are:

1) Transmission Gate Based Master-Slave D Flip Flop

2) True Single-Phase Clock (TSPC) D Flip Flop

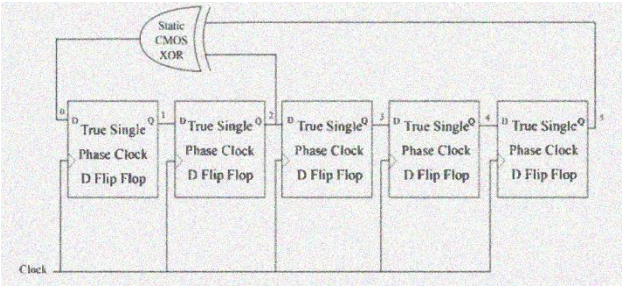
The first architecture takes into account the cascaded master-slave configuration of D Flip Flop. When the clock is "0" the master D - latch is activated and samples the input to the flip flop whereas when the clock is "1" the slave D - latch in activated and passes the value stored by the master to the output. The second architecture uses four inverters which are controlled by the clock. When the clock is at "0" the first inverter samples the inverted D input to its output node and the second inverter is precharged to V_{DD}. The third inverter is OFF and holds the value of the previous inverted D input. When the clock transitions from "0" to "1" the output of the second inverter is passed to the third inverter which gets ON and the fourth inverter is used to get the non-inverted input D. Similarly, two different architectures are presented for the X-OR gate as well:

1) EX-OR Implementation in Static CMOS Logic Style
2) Transmission Gate EX-OR Gate

In the first method, twelve transistors are used from which eight transistors are for the X0R gate and the other two transistors each for two inverters. Whereas the second method needs only six transistors in all.

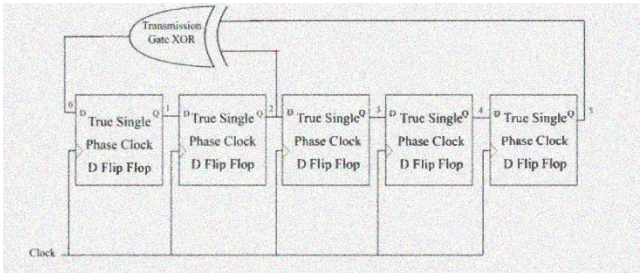
All the above four architectures are explained in detail with the respective diagrams in the paper. Using the amalgamation of the above discussed two architectures each of D flip flop and XOR gate, four designs of LFSR are presented.

a) Implementation of LFSR using TSPC Positive Edge Triggered D Flip Flop and Static CMOS EX-OR



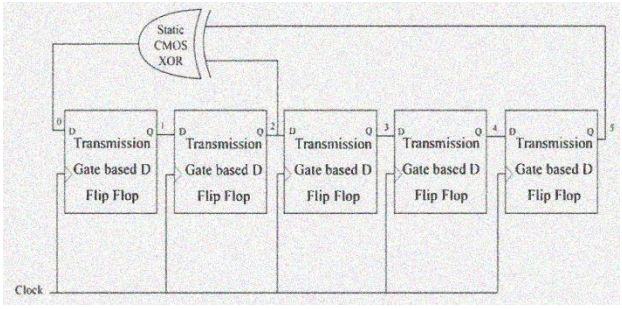
LFSR using TSPC Positive Edge Triggered D Flip Flop and Static CMOS EX-OR Fig.3.3 [2]

b) Implementation of LFSR using TSPC based positive edge-triggered D Flip Flop and transmission gate based EX-OR gate.



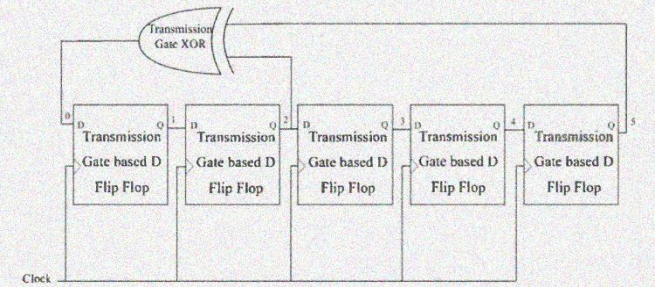
LFSR using TSPC based positive edge-triggered D Flip Flop and transmission gate based EX-OR gate Fig 3.4 [2]

c) Implementation of LFSR using transmission gate master-slave positive edge-triggered D Flip Flop and Static CMOS EX-OR.



LFSR using transmission gate master-slave positive edge-triggered D Flip Flop and Static CMOS EX-OR Fig 3.5 [2]

d)Implementation of LFSR using the transmission gate-based implementation of both D Flip Flop and EX-OR gate.



LFSR using the transmission gate-based implementation of both D Flip Flop and EX-OR gate. Fig 3.6 [2]

A comparison of the highest operating frequency and its corresponding power consumption of all the proposed architectures are shown in the paper. The functionality of all the proposed architectures is verified in the SPICE simulation.

C. MUX based LFSR

[3] proposed a multiplexer based low power design technique for testing. This method explained and illustrated when input change patterns generated by a gray code generator and a counter are EX-ORed along with the seed generated by multiplexer based on LFSR. Low power can be achieved better when single input change generators are used. The paper focuses on reducing the switching activities in the test patterns by replacing an EX-OR gate with a multiplexer. This MUX-LFSR consists of other logical circuits like m-bit counter, gray counter, NOR-gate structure, and EX-OR -array. The m bit counter generates 2m test pattern sequences when initialized with all zeros. The output of m bit counter is directly fed to the gray code generator and NOR gate. The NOR gate output is one only when the output of the counter is all zero which activates LP-LFSR to generate the next seed. The seed from MUX-LFSR and data from gray code generator are EX-ORed and the output is the final output pattern.

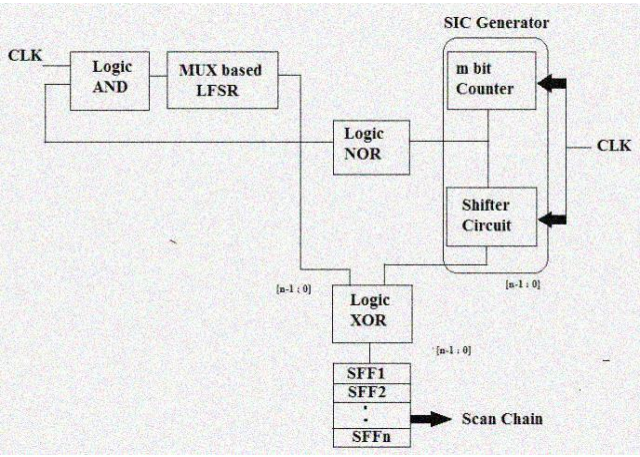


Fig. 3.7 Low Power Test Pattern Generator [3]

The paper also discusses in brief about the Array Multipliers. At last, the paper is concluded with a comparison between EX-OR LFSR and MUX-LFSR in terms of power consumption.

III. DESIGN REVIEW AND RESULT ANALYSIS

A. *For low transition LFSR method[1]*

EDA Tool: Xilinx Product Version: ISE 13.1 Target Device: xc6slx16-3csg324		
Parameter	Type of Random Sequence generator	
	32-bit LFSR	32-bit LT-LFSR
No. of Slices Register	32	28
No. of LUT's	12	9
No. of bounded IOBs	34	36
Total Power (mW)	49.00	23.00
Latency (ns)	3.668	5.194

Table I: Comparison Conventional for LFSR and LT-LFSR [1]

While testing the device, ultimately there is a reduction in power due to a decrease in the number of transitions. Hence power is consumed more efficiently in LT-LFSR as a transition between two successive test patterns is reduced. For the experimental simulation, they used the expression $X^{32}+X+1$ for both LT-LFSR and LFSR to generate 32-bit different test patterns. The results show that the total power is 50.06% less than conventional LFSR.

B. *For Subthreshold LFSR Technique[2]*

Proposed Architecture	Power Consumed at 0.181 MHz (nW)
1	73.3
2	69.9
3	211.7
4	196.2

Table II:Power Consumption at Frequency 0.181MHz [2]

The characteristic polynomial $x^5 + x^2 + 1$ is chosen. The maximal length of 5-bit LFSR is $2^5-1=31$, that is the reason LFSR covers all possible states in 31 clock cycles. All the four proposed architectures are compared in terms of power consumption using power simulation. A common frequency of 0.181 MHZ is taken into consideration. It can be noted from the table that architecture-2 LFSR consumes the least power of 69.9 nW,

followed by the architecture-1 LFSR at 73.3 nW. Architecture 3 and architecture 4 have higher power consumption. The paper also highlights that even though architecture 2 has low power dissipation, architecture 1 is also compatible to operate at double the frequency of former. Hence, depending on the priority of the desired application i.e. low power consumption or high-speed operation, any of the two architectures constructed with TSPC D Flip Flop can be used.

C. *For MUX Based LFSR[3]*

The conclusion is drawn from the comparison of different parameters like area, power consumption, and performance between normal EX-OR based LFSR and Multiplexer based LFSR. Keeping the clock frequency, the same for both the architecture it is noted that the proposed method is better in terms of area, usage and power. The dynamic power is reduced from 113 mW to 107 mW, though the static power remains constant. Logic elements in the circuit are downed to 125 from 127. The paper shows simulation at 113.4 MHZ frequency using Xilinx and X Power analyzer Tool. Using this method power is reduced in the range of 6% to 23%.

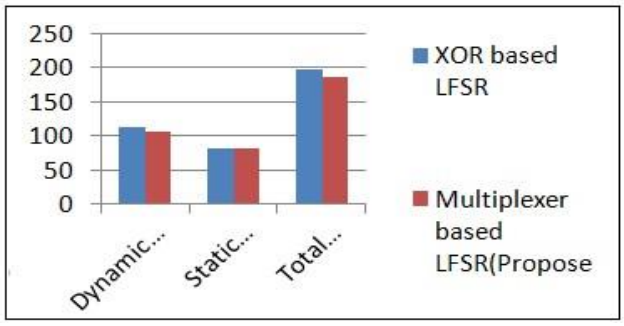


Fig.4 Power Analysis [3]

IV. CONCLUSION

After reviewing all the above-mentioned techniques, the low transition technique reflects power reduction up to 50.06% compared to conventional LFSR. Moreover, the Mux-based LFSR technique brings a little power reduction ranging from 6% to 23% without affecting its clock frequency. Using LFSR in the sub-threshold region, it corresponds to better power reduction in the highest operating frequency. To conclude, in case of low frequency, the sub-threshold techniques using different structures of EX-OR and D Flip Flop is a better option to implement. The Mux-based LFSR is very helpful especially in testing IoT Hub devices. But low transition LFSR technique reduces the highest amount of power dissipation. All the three papers taken into consideration propose different ideas to reduce the power consumption while testing the chip

REFERENCES

1. Tejas Thubrikar, Sandeep Kakde, Shweta Gaidhani, Shailesh Kamble and Nikit Shah Design and Implementation of Low Power Test Pattern Generator Using Low Transitions LFSR ("International Conference on Communication and Signal Processing, April 6-8, 2017, India", Publisher :IEEE)
2. Kirti Gupta , Prayanshu Sharma and Neeta Pandey Design of Low Power Subthreshold Linear Feedback Shift Registers ("1st IEEE International Conference on Power Electronics. Intelligent Control and Energy Systems (ICPEICES-2016")

3. Dr Sabir Hussain Design of Low Power Multiplexer based LFSR for testing IoT Devices (“Journal of Information and Computational Science – 2019”)
4. Roshni Oommen, Merin K George, Sharon Joseph Study and Analysis of Various LFSR Architectures (“©2018 IEEE”)
5. Jayasanthi M, Kowsalyadevi AK Low Power Implementation of Linear Feedback Shift Registers (“International Journal of Recent Technology and Engineering (IJRTE)-2019”)
6. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design , Tata McGraw-Hill, 2003
7. PrasadaRao, R. Vara, N. Anjaneya Varaprasad, G.
8. Sudhakar Babu, and C. Murali Mohan. "Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power
9. BIST implemented in HDL." International Journal of Modern Engineering Research (IJMER) 3, no. 3 (2013): 1523-1528.
10. A.Kavitha,G.Seetharaman, and T.N.Prabhakar,Shrinithi Design of Low Power TPG using LP/LFSR”, 3rd IEEE Conference on international conference on intelligent systems modeling and simulation,2012